IN THE CLAIMS:

1. (currently amended) For use in a wide-issue pipelined processor, a mechanism for reducing pipeline stalls between conditional branches, comprising:

~~a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in a pipeline of said processor; and~~

mispredict program counter (PC) ~~PC~~ storage~~, coupled to said mispredict PC generator and including a mispredict PC queue and a number of staging registers~~, configured to store multiple mispredict PC values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction in a pipeline of said processor; and

a mispredict PC value selector configured to select one of said multiple mispredict PC values to track a corresponding conditional branch instruction as said corresponding conditional branch instruction moves through stages of said pipeline, said select based on when said corresponding conditional branch instruction enters said pipeline

~~that stores said mispredict PC value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said processor if said resolution results in a mispredict condition~~

~~, said mispredict PC queue having at least as many slots as said number of said staging registers~~.

2. (currently amended) The mechanism as recited in Claim 1 further comprising a mispredict PC generator configured to generate a mispredict PC value for each conditional branch instruction in said pipeline ~~is associated with a static branch predictor of said processor~~.

3. (currently amended) The mechanism as recited in Claim 2 ~~1~~ wherein said mispredict PC generator generates a branch prediction employed to prefetch instructions and said mispredict PC value in a single clock cycle.

4. (currently amended) The mechanism as recited in Claim 1 ~~3~~ wherein said mispredict PC storage includes a number of staging registers and a mispredict PC queue configured to store said multiple mispredict PC values, said mispredict PC value selector configured to select said one of said multiple mispredict PC values from said mispredict PC queue to cause said selected one to move into said staging registers to track said corresponding conditional branch instruction ~~branch prediction is employed to prefetch instructions~~.

5. (canceled)

6. (currently amended) The mechanism as recited in Claim 1 wherein said one of said multiple mispredict PC values tracks said corresponding conditional branch instruction by moving ~~value moves~~ through ~~said~~ staging registers of said mispredict PC storage as said corresponding conditional branch instruction moves through said stages in said pipeline.

7. (currently amended) The mechanism as recited in Claim 1 wherein said mispredict PC storage stores said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction ~~resolution~~ occurs in an execution stage of said pipeline.

8. (currently amended) The mechanism as recited in Claim 2 ~~1~~ wherein said mispredict PC generator is configured to generate said mispredict PC value before branch instructions are grouped ~~processor is a digital signal processor~~.

9. (currently amended) For use in a wide-issue pipelined processor, a method of reducing pipeline stalls between conditional branches, comprising:

~~generating a mispredict program counter (PC) value for each conditional branch instruction in a pipeline of said processor;~~

~~using a number of staging registers to align said mispredict PC value with said conditional branch instruction in said pipeline;~~

storing multiple ~~said~~ mipredict program counter (PC) values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction in a pipeline of said processor ~~PC value in a mispredict PC queue having at least as many slots as said number of said staging registers~~;

selecting one of said multiple mispredict PC values to track a corresponding conditional branch instruction as said corresponding conditional branch instruction moves through stages of said pipeline; and

basing said selecting on when said corresponding conditional branch instruction enters said pipeline

~~storing said mispredict PC value at least until a resolution of said conditional branch instruction occurs; and~~

~~making said mispredict PC value available to a PC of said processor if said resolution results in a mispredict condition~~.

10. (currently amended) The method as recited in Claim 9 further comprising generating a ~~wherein said~~ mispredict PC value for each conditional branch instruction in said pipeline ~~generator is associated with a static branch predictor of said processor~~.

11. (currently amended) The method as recited in Claim 10 ~~9~~ wherein said generating is carried out in a single clock cycle, said method further comprising generating a branch prediction in a single clock cycle.

12. (currently amended) The method as recited in Claim 9 ~~11~~ wherein said selecting includes selecting one of said multiple mispredict PC values from a mispredict PC queue configured to store said multiple mispredict PC values ~~further comprising employing said branch prediction to prefetch instructions~~.

13. (canceled)

14. (currently amended) The method as recited in Claim 9 wherein said one of said multiple ~~further comprising moving~~ mispredict PC values tracks said corresponding conditional branch instruction by moving ~~value~~ through ~~said~~ staging registers in a ~~said~~ mispredict PC storage as said corresponding conditional branch instruction moves through stages in said pipeline.

15. (currently amended) The method as recited in Claim 9 wherein said storing includes storing said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction ~~resolution~~ occurs in an execution stage of said pipeline.

16. (original) The method as recited in Claim 9 wherein said processor is a digital signal processor.

17. (currently amended) A digital signal processor, comprising:

a pipeline having stages capable of executing conditional branch instructions;

a wide-issue instruction issue unit;

~~a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in said pipeline; and~~

mispredict program counter (PC) ~~PC~~ storage~~, coupled to said mispredict PC generator and including a mispredict PC queue and a number of staging registers,~~ that stores multiple ~~said~~ mispredict PC values, wherein each of said multiple mispredict PC values corresponds to a conditional branch instruction in said pipeline; and

a mispredict PC value selector that selects, based on when said corresponding conditional branch instruction enters said pipeline, one of said multiple mispredict PC values to track said corresponding conditional branch instruction as said corresponding conditional branch instruction moves through said stages

~~value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said DSP if said resolution results in a mispredict condition, said mispredict queue having at least as many slots as said number of said staging registers~~.

18. (currently amended) The DSP as recited in Claim 17 further comprising a ~~wherein said~~ mispredict PC generator that generates a mispredict PC value for each conditional branch instruction in said pipeline ~~is associated with a static branch predictor in said instruction issue unit~~.

19. (currently amended) The DSP as recited in Claim 18 ~~17~~ wherein said mispredict PC generator generates a branch prediction employed to prefetch instructions and said mispredict PC value in a single clock cycle.

20. (currently amended) The DSP as recited in Claim 19 wherein said mispredict PC storage includes a number of staging registers and a mispredict PC queue that stores said multiple mispredict PC values, said mispredict PC value selector configured to select said one of said multiple mispredict PC values from said mispredict PC queue to cause said selected one to move into said

staging registers to track said corresponding conditional branch instruction ~~branch prediction is employed to prefetch instructions~~.

21. (canceled)

22. (currently amended) The DSP as recited in Claim 17 wherein said one of said multiple mispredict PC values tracks said corresponding conditional branch instruction by moving ~~value moves~~ through ~~said~~ staging registers in said mispredict PC storage as said corresponding conditional branch instruction moves through said stages.

23. (currently amended) The DSP as recited in Claim 17 wherein said mispredict PC storage stores said each of said mispredict PC values at least until a resolution of said corresponding conditional branch instruction and said resolution occurs in an execution stage of said pipeline.

24. (currently amended) The mechanism as recited in Claim 4 ~~1~~ wherein said mispredict PC queue of said mispredict PC storage has at least one more slot than said number of said staging registers.

25. (currently amended) The method as recited in Claim 12 ~~9~~ wherein said mispredict PC queue of said mispredict PC storage has at least one more slot than a ~~said~~ number of ~~said~~ staging registers employed with said storing.

26. (currently amended) The DSP as recited in Claim 20 ~~17~~ wherein said mispredict PC queue of said mispredict PC storage has at least one more slot than said number of said staging registers.